

Re: HEADSUP: New i386 interrupt and SMP code..

Source: <http://unix.derkeiler.com/Mailing-Lists/FreeBSD/arch/2003-11/0003.html>

From: John Baldwin (jhb_at_FreeBSD.org)

Date: 11/03/03

Date: Mon, 03 Nov 2003 11:29:43 -0500 (EST)
To: Jeff Roberson <jroberson@chesapeake.net>

On 02-Nov-2003 Jeff Roberson wrote:

>
> *On Thu, 30 Oct 2003, John Baldwin wrote:*
>
>> *Coming very soon to a CVS tree near you are some very large changes to*
>> *the i386 interrupt and SMP code. New features include:*
>>
>> *- Runtime selection of using the I/O APICs or the AT PICs to route*
>> *interrupts.*
>> *I/O APICs can be used in a UP kernel or on a UP system that*
>> *supplies either an MP Table or ACPI APIC Table.*
>> *An SMP kernel can run on a UP machine. This means that SMP*
>> *can now be enabled in GENERIC and the SMP kernel config can die.*
>
> *The lock prefix is extremely expensive on the P4 systems that I have*
> *measured. It makes lock cpxchg 150 cycles vs 12. On athlon this is not*
> *such a big deal since it goes to 25 cycles from 12. We should measure the*
> *impact of compiling in the lock prefix on UP P4 systems before making this*
> *the default.*
>
> *Otherwise, this all sounds good.*

Note that one can always compile a custom kernel if one needs it for a specific application, but that this will increase the amount of out-of-box support for i386. This has also been a requested feature for quite a while now.

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