

Re: fast ethernet driver MII phy serial clock rates

Source: <http://unix.derkeiler.com/Mailing-Lists/FreeBSD/net/2004-04/0217.html>

From: Mike Silbersack (*silby_at_silby.com*)

Date: 04/24/04

Date: Sat, 24 Apr 2004 14:04:14 -0500 (CDT)

To: David Burns <david.burns@dugeem.net>

On Sat, 24 Apr 2004, David Burns wrote:

> *Hello all,*
>
> *It appears that quite a few of the "el cheapo" hardware Fast Ethernet*
> *drivers (at least rl, sis, ste, vr, wb – these are just the ones I found*
> *in /usr/src/sys/pci) have added DELAY(1) statements around MII serial*
> *clock ops which will result in a max Management Data Clock (MDC)*
> *frequency of 500kHz for the serial management interface. Which means*
> *that a mii_readreg (or writereg) operation will take a minimum of 128?s*
> *(64?s for mii_sync + 64?s for data read/write). During which time the*
> *driver is locked.*

This is an old problem, most of us leave it alone because hardware can break in strange ways. :)

> *NB this assumes that a DELAY(1) is really a delay of 1?s! Which I don't*
> *think it is ... :-(*

Correct, DELAY takes far longer than it should.

If you're really interested in fixing the problem and not inadvertently breaking older cards, what you should do is implement a nanodelay function that actually delays for the time it's supposed to and then delay the rated amount. Removing all delays will probably break something somewhere.

Mike "Silby" Silbersack

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